CALCULATED PERFORMANCE OF S.I.S. JUNCTIONS AS FREQUENCY MULTIPLIERS

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ABSTRACT

The harmonic balance technique is applied to examine the performance of SIS junctions as millimeter- and submillimeter-wave frequency multipliers. The effects of drive level, bias, embedding impedance, and junction parameters on harmonic generation are described. The calculations show that the output power is only a few nanowatts per junction, but that the efficiency is reasonable: in the range of 15-18% for realistic junction parameters.

INTRODUCTION

Superconductor-insulator-superconductor (SIS) junctions are now the preferred devices for low noise millimeter-wave and submillimeter-wave mixers, due mainly to the strong nonlinearity in their current-voltage characteristic, which is comparable to the quantum energies at the pump and signal frequencies. In this paper we examine the possibility of using this same nonlinearity for frequency multiplication. Although the absolute power levels for SIS junctions are very low, the presence of nonlinear reactance leads one to suppose that the conversion efficiency for an SIS multiplier might be reasonably good, so that the devices could be useful if placed in a power combining array. The calculations presented here show the dependence of the conversion efficiency and output power on pumping level, bias, embedding impedances, IV curve rounding, and subgap leakage.

ANALYSIS METHOD

Accurate analysis of a circuit containing an SIS junction requires a self-consistent large-signal solution for the voltage across the nonlinear device . In the method used here, several simplifying (but not unrealistic) assumptions are made: (1) The Josephson effect is not included. In a practical multiplier this would mean that the effect is suppressed by an external magnetic field. (2) Self-oscillation and other nonharmonic frequency generation effects are ruled out. (3) The Fourier series for the voltage is terminated after a finite number of harmonics. In practice this is satisfied because of the shorting action of the junction capacitance.

DC IV Curve and Response Function

The algorithm described below can be applied directly to experimental IV curves; but for the purposes of this study the unpumped current-voltage characteristic $I_{dc}(V)$ was modeled using five parameters: V_g, the junction gap voltage; R_N, the normal resistance; R_L, the leakage resistance; and V' and V", two sharpness parameters describing the rounding of the IV curve at the top and bottom of the current rise at V_g. For $0 < V < Vg$,

$$I_{dc} = V/R_L + \left[(1/R_N - 1/R_L)(V_g/V' + 1) \cdot \frac{1}{\Delta}\left(\exp\{(V - V_g)/V'\} - \exp\{-V_g/V'\}\right)\right] \quad (1a)$$

while for $V > Vg$,

$$I_{dc} = V/R_N + \left[(1/R_N - 1/R_L)(1 - \exp\{-V_g/V'\} - V_g/V') \cdot \frac{1}{\Delta}\exp\{(V_g - V)/V''\}\right] \quad (1b)$$

where

$$\Delta = \frac{1}{V''}(1 - \exp\{-V_g/V'\}) + \frac{1}{V'} \quad (1c)$$

To cover $V < 0$, the current is assumed to be an odd function of voltage. A typical IV curve is plotted in Figure 1; the current and its first derivative are continuous at the origin and at V_g.

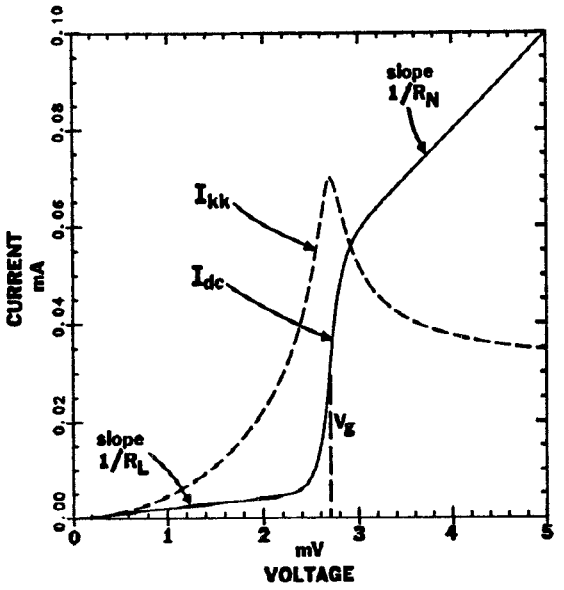

Figure 1: Plot of dc IV Curve model as given in equation (1) (the solid line), with its Kramers-Kronig transform (the dashed line). V_g = 2.7 mV, V' = V" = 0.1 mV, R_N = 50 ohms, R_L = 500 ohms.

Due to quantum effects, the instantaneous current through the junction cannot be determined directly from the IV curve alone. Instead, as described in the next section, the current depends on a phase factor W(t), and on a response function $r(V) = I_{kk} + jI_{dc}$ where I_{kk} is the Kramers-Kronig transform with respect to voltage of I_{dc} with the ohmic part subtracted out (that is, $I_{dc} - V/R_N$) [1].

Harmonic Balance

In the well known harmonic balance method, a self-consistent solution is obtained by finding a Fourier series for the voltage, such that the resulting currents through the nonlinear junction and the linear embedding circuit match at each harmonic. Several methods are available for obtaining harmonic balance; we have used an iteration/relaxation method similar to that used by Hicks and Khan [2] and applied to SIS mixers by Hicks, Feldman, and Kerr [3]. It consists of a three step iteration.

Step 1 (Nonlinear Part): Given an initial trial solution for the voltage V(t), the corresponding current I(t) through the junction is given by [1]:

$$I(t) = \mathrm{Im} \int_{-\infty}^{\infty}\int W(\omega')\, W(\omega'') \exp\{-j(\omega' - \omega'')t\} \cdot r(V_o + h\omega'/e)\, d\omega'\, d\omega'' \qquad (2a)$$

where

$$W(t) = \exp\left\{\frac{-je}{h}\int^{t} [V(t') - V_o]\, dt'\right\} \qquad (2b)$$

and $W(\omega)$ is the Fourier transform of the phase factor W(t). As stated above, this current does not include the Josephson effect. It also does not include the current due to the junction capacitance, which is instead included as part of the linear embedding circuit.

Rather than evaluate the above expressions through numerical integration or a product-of-Bessel-functions expansion, we represent the both the voltage V(t) and the phase factor W(t) by complex Fourier series, with coefficients V_n and W_n, respectively. The W_n can be found efficiently through the use of FFT routines. First, the V_n are divided by $jn\omega_o$ to carry out the time integration in the argument of (4); the zero order term is set to zero. An inverse FFT converts the Fourier series to a time series, which is then multiplied by -je/h and exponentiated, leaving a time series for the phase factor. A forward FFT is then applied to give the W_n. It should be noted that W(t) is a complex function of time, so that W_{-n} does not necessarily equal W^*_n. The series for the phase factor is substituted into (2a), the result is

$$I(t) = \mathrm{Im} \sum_m \sum_n W_m W^*_{m+n} e^{jn\omega_o t}\, r(V_o + hm\omega_o/e) \qquad (3)$$

I(t) is evaluated at a number of sample points; an inverse FFT then yields the harmonic current coefficients I_n.

For ordinary embedding circuits, with pump voltages up to two or three times the fundamental quantum step $h\omega_o$, sixteen points (seven harmonics) carried through the computations are sufficient to get 0.1% accuracy in the final results. For larger pump voltages, or when one is interested in the high-order harmonics, 32 or 64 points may be necessary.

Step 2 (Linear Part): The linear embedding circuit is defined to include the junction capacitance as well as the external source, load, and idler impedances. The voltage across the linear circuit is:

$$V_n^{lin} = \begin{cases} -I_nZ_n + V_d/2 & n = +/- 1 \\ -I_nZ_n + V_{bias} & n = 0 \\ -I_nZ_n & \text{otherwise} \end{cases} \qquad (4)$$

where V_{bias} is the bias voltage, V_d is the peak drive voltage, and Z_n is the impedance of the embedding circuit at the n-th harmonic, positive or negative ($Z_{-n} = Z_n^*$).

Step 3 (Voltage Update): When a self-consistent set of voltage harmonics has been obtained, the V_n^{lin} found in step 2 should match the initial guess in step 1 above. If the two do not match closely, a new guess is made:

$$V_n^{new} = p_n V_n^{lin} + (1 - p_n)\, V_n^{old} \qquad (5)$$

for all n, where the p_n are relaxation constants, with $|p_n| \le 1$, and the procedure is repeated from step 1. The iteration process is continued until convergence to the desired accuracy is obtained. In the test cases tried, V_n=0 for all n was found to be a satisfactory guess for the initial trial voltage, and $p_n = R_N/(Z_n + R_N)$ to be a good value for the relaxation constants. Convergence to six decimal places is typically obtained within 20 iterations.

RESULTS

For the calculations presented here, we assumed a "typical" junction with parameters V_g = 2.7 mV, R_N = 50 ohms, R_L = 500 ohms, and V' = V" = 0.1 mV, unless otherwise noted. These numbers model commercially available Nb-Al_2O_3-Nb junctions, 1 micron square. It was found that the power levels obtainable from devices of this type are very low: on the order of a few nanowatts harmonic power for a few tens of nanowatts of pumping power. On the other hand, the efficiencies are reasonably good: in the range of 15-18% for doublers and 5 -10% for triplers. These numbers would increase considerably if V', V", and R_L could be improved. The power available from a single junction, assuming proper terminations and drive levels, is approximately proportional to its area; in a power combining multiplier, the total power would be proportional to the sum of the junction areas.

Optimum Pumping Level and Bias

Figure 2 shows the dependence of conversion efficiency on the ac pumping voltage across the device and the dc bias voltage, for an SIS junction doubling from 80 to 160 GHz. The peaks are separated in bias voltage by roughly the quantum step ($h\omega_o$). As the bias voltage changes, the optimum pumping amplitude also changes, increasing as the bias moves farther from the gap voltage. The optimum bias point for an n-th order multiplier is roughly n-1 quantum steps below the gap voltage; since n-1-th order mixing is closely related to n-th order multiplying, this could imply that an n-th order harmonic mixer should be biased roughly n quantum steps below the gap.

The highest efficiency (13.2% in the particular case shown) is at the n-1-th peak below the gap voltage. However, the highest output power is obtained farther out on the efficiency 'ridge', with lower bias and higher pumping.

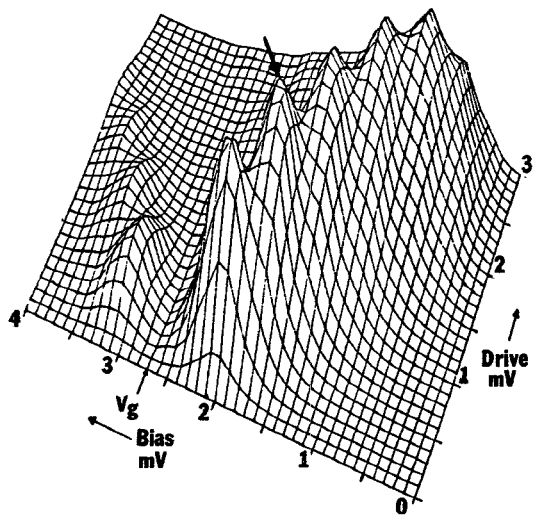

Figure 2: Conversion efficiency vs. peak pump voltage and dc bias for a single junction doubler from 80 GHz to 160 GHz. The peak indicated in this case is 13.2%.

Large Signal Impedance

For good coupling of pumping power to the junction it is useful to know its effective large signal impedance at the pump frequency. This is shown (not including junction capacitance), as a function of drive level, in Figure 3. There is a significant difference between the small signal impedance and the large signal impedance, which becomes mostly resistive with a value about equal to the normal resistance for levels several times the quantum step. This data indicates that a simple large signal model for matching to the device at the fundamental frequency is simply R_N in parallel with the geometric junction capacitance.

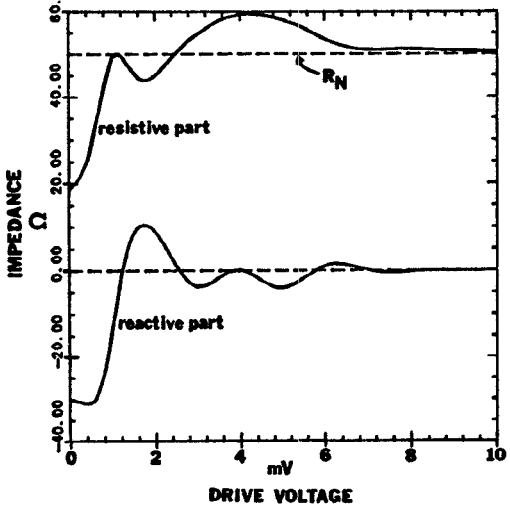

Figure 3: Large signal impedance of an SIS junction vs. pumping voltage at 80 GHz, with higher harmonics shorted, and not including geometric junction capacitance. The value at zero pump represents the small signal impedance.

Variations in the embedding impedance presented to the device at the harmonic frequencies have an effect on the impedance presented by the device to the pumping source. Figure 4 shows a plot of second harmonic impedance superimposed on the resulting fundamental impedance.

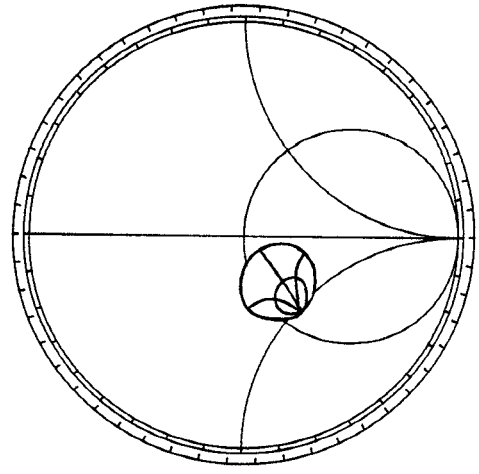

Figure 4: Effect of second harmonic termination on large-signal impedance presented by diode at fundamental frequency. The small Smith chart is the second harmonic impedance; the values on the large chart underneath are the corresponding large signal impedances. Both are normalized to the normal resistance R_N. Fundamental frequency is 80 GHz, the pump is 1.9 mV peak, and the dc bias 1.0 mV.

Optimum Load Impedance

In Figure 5 (next page) we show the effects of changing the embedding impedance at the desired harmonic frequency (including the junction capacitance) on the efficiency of a doubler. The impedance charts are normalized to R_N, which appears to be approximately the optimum. The fact that the optimum impedance is purely real indicates that a tuning structure to resonate out the junction capacitance is necessary for effective multiplication.

Optimum Idler Impedances

Proper termination of the idler frequencies (harmonics other than the desired one) improves multiplier performance. As one would expect, our calculations show that the optimum idler impedances are purely reactive, and that the effect of the third harmonic termination in a doubler (Figure 6a) is weaker than the effect of the second harmonic termination in a tripler (Figure 6b). In both cases the magnitude of the best reactance is approximately equal to the normal resistance.

Effect of IV Curve Sharpness and Subgap Leakage

A "sharp" IV curve is important for good harmonic generation, and the typical values of V' and V" for currently available junctions are far greater than the small values needed for optimum conversion, as illustrated by Figure 7. It appears that reductions in V' and V" could improve the performance of a doubler by a factor of two.

Calculations of the effect of the subgap leakage show that increasing the leakage resistance improves the efficiency.

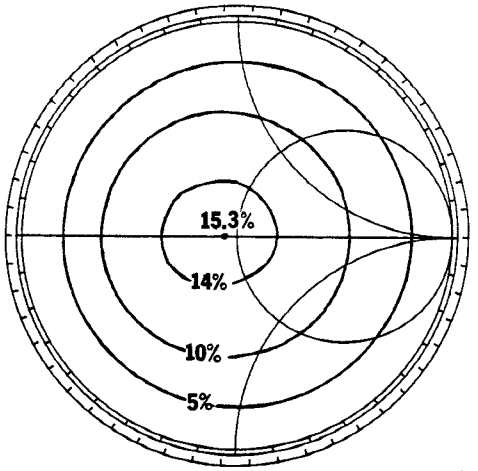

Figure 5: Effect of second harmonic termination on efficiency of an 80 to 160 GHz doubler, with drive level and bias held constant. The chart is normalized to R_N. The optimum is real and slightly less than the normal resistance.

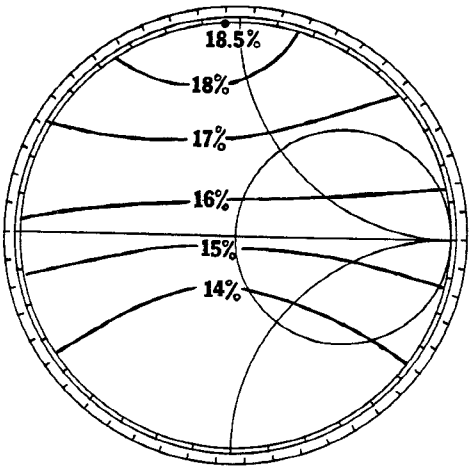

Figure 6a: Effect of third harmonic idler termination on efficiency of a 80 to 160 GHz doubler. The optimum impedance is purely reactive.

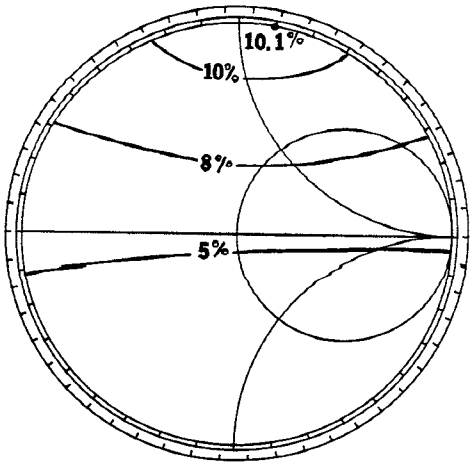

Figure 6b: Effect of second harmonic idler termination on efficiency of a 80 to 240 GHz tripler. This shows the importance of proper termination of the lower order frequencies in a high order multiplier.

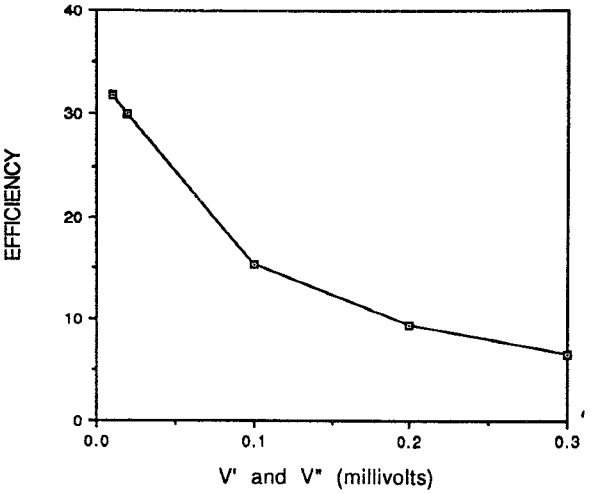

Figure 7: Effect of IV curve sharpness on doubler efficiency; smaller values of V' and V" give a more abrupt current rise at V_g. V' and V" were varied simultaneously; the other parameters were held constant.

APPLICATIONS

The low power levels and the need for cryogenic cooling are major disadvantages of SIS frequency multipliers compared to conventional varactor multipliers. However, the SIS devices have an advantage in that large numbers of them can be more easily integrated into planar arrays, thus allowing simple power combining, and that the parasitic resistances associated with whisker-contacting can be eliminated, thus allowing simple operation at submillimeter wavelengths. One obvious application for SIS multipliers would be as a local oscillator source for SIS mixers, which need very low LO power and already require a cryogenic system.

It should be noted that the procedures described here could be easily applied to SIN or super-Schottky devices by making appropriate changes in the dc IV curve parameters.

ACKNOWLEDGMENTS

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REFERENCES

[1] J.R.Tucker and M.J.Feldman, "Quantum detection at millimeter wavelengths," Reviews of Modern Physics, vol.57, no.4, Oct. 1985, pp. 1055-1113.

[2] R.G. Hicks and P.J.Khan, "Numerical analysis for determining pumped nonlinear device waveforms," IEEE Transactions on Microwave Theory and Techniques, vol. MTT-30, no.3, Mar.1982, pp.251-259.

[3] R.G.Hicks, M.J.Feldman, and A.R.Kerr, "A general numerical analysis of the superconducting quasiparticle mixer," IEEE Transactions on Magnetics, vol. MAG-21, no.2, Mar. 1985, pp.208-211.